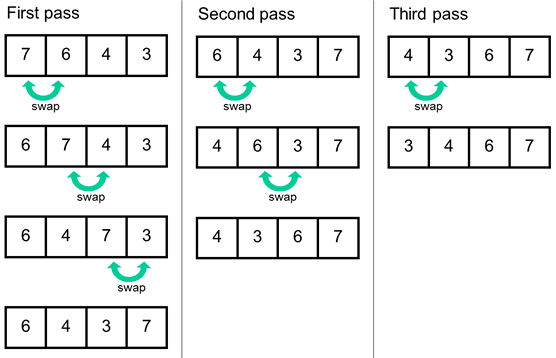
**數位系統導論期末範例5**

**Bubble Sort演算法離散事件建模和電路合成**

**陳慶瀚**

**2022-06-08**

**1. Bubble Sort演算法**



**C Code**

unsigned char rama[10]={1,3,5,7,9,2,4,6,8,0};  
unsigned char terapl;  
unsigned char terap2,  
for(int i=0;i<10;i++)  
{  
 terapl=rara[i];  
 for(int j=i+1;j<10;j++)  
 {  
 terap2=rara[j];  
 if(terapl>terap2)  
 {  
 rara[i]=terap2;  
 rara[j]=terapl;  
 terapl=terap2,  
 }  
 }

}

**2. GRAFCET建模**



**控制器電路合成**

**grafcet: process(CLK,RST)**

**begin**

**if RST='0' then**

**X0<='1';X1<='0';X2<='0';**

**X3<='0';X4<='0';X5<='0';**

**X6<='0';X7<='0';X8<='0';**

**X9<='0';**

**elsif CLK'event and CLK='1' then**

**if X0='1' and START='1' then X0<='0';X1<='1';**

**elsif X1='1' then X1<='0';X2<='1';**

**elsif X2='1' then X2<='0';X3<='1';**

**elsif X3='1' and (temp1 > temp2) then X3<='0';X4<='1';**

**elsif X3='1' and (temp1 <=temp1) then X3<='0';X5<='1';**

**elsif X4='1' then X4<='0';X5<='1';**

**elsif X5='1' then X5<='0';X6<='1';**

**elsif X6='1' and (j<10) then X6<='0';X2<='1';**

**elsif X6='1' and (j>=10) then X6<='0';X7<='1';**

**elsif X7='1' then X7<='0';X8<='1';**

**elsif X8='1' and (i<9) then X8<='0';X1<='1';**

**elsif X8='1' and (i>=9) then X8<='0';X9<='1';**

**elsif X9='1' and START='0' then X9<='0';X0<='1';**

**end if;**

**end if;**

**end process;**

**Datapath電路合成**

**datapath: process(CLK,RST)**

**begin**

**if CLK'event and CLK='1' then**

**if X0='1' then i<=0;FINISH<='0';**

**elsif X1='1' then temp1<=ram(i);j<=i+1;**

**elsif X2='1' then temp2<=ram(j);**

**elsif X4='1' then ram(i)<=temp2;ram(j)<=temp1;temp1<=temp2;**

**elsif X5='1' then j<=j+1;**

**elsif X7='1' then i<=i+1;**

**elsif X9='1' then FINISH<='1';**

**end if;**

**end if;**

**end process;**

**系統合成**

**LIBRARY IEEE;**

**USE IEEE.STD\_LOGIC\_1164.all;**

**USE IEEE.STD\_LOGIC\_ARITH.ALL;**

**USE IEEE.STD\_LOGIC\_UNSIGNED.ALL;**

**entity bubble\_sort is**

**port(**

**clk,rst,START : in std\_logic;**

**FINISH :out std\_logic;**

**r0,r1,r2,r3,r4,r5,r6,r7,r8,r9 : out integer range 0 to 15**

**);**

**end bubble\_sort;**

**architecture arch of bubble\_sort is**

**signal X0,X1,X2,X3,X4,X5,X6,X7,X8,X9 : std\_logic;**

**signal temp1,temp2 : integer range 0 to 15;**

**signal i,j : integer range 0 to 15;**

**type ram\_type is array (0 to 9) of integer range 0 to 15;**

**signal ram: ram\_type :=(1,3,5,7,9,2,4,6,8,0);**

**begin**

**grafcet: process(CLK,RST)**

**begin**

**……**

**end process;**

**datapath: process(CLK,RST)**

**begin**

**……**

**end process;**

**r0 <= ram(0);**

**r1 <= ram(1);**

**r2 <= ram(2);**

**r3 <= ram(3);**

**r4 <= ram(4);**

**r5 <= ram(5);**

**r6 <= ram(6);**

**r7 <= ram(7);**

**r8 <= ram(8);**

**r9 <= ram(9);**

**end arch;**

**波形模擬**

